

### **Remarks**

Claims 1-3 and 5-9 are pending in the application. Claims 1, 3, 6 and 8 have been amended herein. Favorable reconsideration of the application, as amended, is respectfully requested.

#### ***I. REJECTION OF CLAIMS 1, 3 AND 6-9 UNDER 35 USC §103(a)***

Claims 1, 3 and 6-9 stand rejected under 35 USC §103(a) based on U.S. Patent No. 5,982,887 (*Hirofani*) in view of U.S. Patent No. 6,907,125 (*Oishi*) in further view of Applied Cryptography (*Schneier*). Withdrawal of the rejection is respectfully requested for at least the following reasons.

##### ***A. Using a single circuit for data scramble and error correction***

The Examiner, in addressing applicant's argument that the cited art does not disclose using a single circuit for data scramble and error correction, states that this feature (i.e., a single circuit for data scramble and error correction) is not recited in the rejected claims. Applicants respectfully disagree with the Examiner's interpretation of the claims. Nevertheless, applicants have amended independent claims 1, 3, 6 and 8 to positively recite that the scramble circuit is a single hardware circuit, and that the scramble circuit acts as part of an error correction circuit included in the single hardware circuit.

##### ***B. Oishi does not teach that a data scramble circuit acts as part of an error correction circuit***

In addressing applicant's argument that *Oishi* does not teach a data scramble circuit that acts as part of an error correction circuit, the Examiner states "*Oishi* clearly teaches an error correction system in which the error correction codes are decoded by a decryption circuit prior to the decrypted codes being used to correct errors." The Examiner then references Fig. 4 and column 5, lines 37-46 of *Oishi* for support. According to the Examiner, since decryption by the decryption circuit is necessary in order for error correction by the error correction circuit to occur, the decryption circuit acts as part of the error correction circuit. Applicants respectfully disagree with the Examiner for at least the following reasons.

Applicants acknowledge that *Oishi* discloses a decryption circuit 12 and an error decoding circuit 13. However, applicants disagree with the Examiner's reasoning that since the "decryption circuit is necessary in order for error correction by the error correction circuit to occur, the decryption circuit **acts as part of the error correction circuit**", and respectfully submit that this reasoning is flawed as illustrated below.

Fig. 4 of *Oishi* is a flow chart that illustrates the steps of a method, while column 5, lines 37-46 describe the method steps of Fig. 4. Applicants acknowledge that steps 401 and 402, which relate to decrypting data, occur before step 403, which relates to decoding data. However, a method step being performed before another method step does not support a conclusion that one step acts as part of another step. Instead, a more reasonable conclusion is that the steps are independent of one another. If such steps indeed acted as part of another step, as contended by the Examiner, there would be some indication that the steps are interrelated (e.g., a dashed box surrounding the steps). No such indication is found in Fig. 4 or in the cited text.

Further, and with reference to Fig. 1 of *Oishi*, there is shown a block diagram of an information processing apparatus. As can be seen in Fig. 1, the decryption circuit 12 is separate and distinct from the error correcting decoding circuit 13. Of course, the decryption circuit 12 must act before any downstream circuit can react. However, this does not support a conclusion that the down stream circuits act as part of the upstream circuit. They still are independent circuits. For example, the decryption circuit 12 is necessary for the monitor 22 to display information (i.e., the signal provided to the monitor is processed by the decryption circuit). Thus, according to the Examiner's reasoning, the decryption circuit 12 acts as part of the monitor 22. Clearly this is not the case.

If a first process is performed prior to or feeds a second process, it does not follow that the first process acts as part of the second process. Yet this is the reasoning used by the Examiner in rejecting the claims.

Moreover, even if the Examiner's above argument is assumed valid, it is noted that claims 1, 3, 6 and 9 have been amended to positively recite that the scramble circuit is a single

hardware circuit and acts as part of an error correction circuit included in the single hardware circuit. *Oishi* describes an apparatus for processing information including an error correcting coding device and an encryption device. As can be seen in Fig. 1 of *Oishi*, the error correcting coding device and encryption coding device are implemented in different circuits (i.e., ECC circuit 4 and 13, encryption circuit 5 and decryption circuit 12). Moreover, *Oishi* clearly describes the ECC circuits 4, 13, the encryption circuit 5 and the decryption circuit 12 as being separate circuits (see, e.g., col. 4, Ins. 21-25, col. 5, Ins. 4-20, col. 8, lines 37-43 and Figs. 1 and 6). The teachings of *Oishi* must be considered as a whole. Thus, the combination of *Hirofani*, *Schneier* and *Oishi* would result in a circuit having individual decryption and error correcting circuits.

*Oishi* simply does not teach or suggest a scramble circuit that is a single hardware circuit and acts as part of an error correction circuit included in the single hardware circuit, as recited in the independent claims 1, 3, 6 and 8. Rather, *Oishi* teaches directly away from such a combination by teaching that the error correcting coding device and the decryption coding device are implemented in different circuits.

**C. The Examiner cannot pick and choose from the teachings of *Oishi***

In addressing applicant's argument that the Examiner may not pick and choose, the Examiner states that he has merely taken the teachings of *Oishi* regarding error correction and combined them with the decryption of *Hirofani*. The Examiner appears to have misunderstood applicants' previous argument that the Examiner may not pick and choose from the teachings of *Oishi*.

The Examiner admits that *Hirofani* fails to teach a data scramble circuit being a hardware circuit that acts as part of an error correction circuit. The Examiner then contends that *Schneier* teaches a hardware decryption circuit and that *Oishi* teaches that a decryption circuit acts as part of an error correction circuit, and the combination of *Hirofani*, *Oishi* and *Schneier* render claims 1, 3 and 6-9 obvious.

In response, applicants argued that the Examiner cannot pick and choose the portions *Oishi* that are combined with *Hirofani*. Specifically, *Hirofani* teaches decryption while *Oishi* teaches a decryption circuit and error correction circuit as separate circuits. With respect to

picking and choosing, applicants were referring to the fact that *Oishi* must be taken as a whole. In other words, and assuming *Oishi* is combinable with *Hirofani*, the combination must yield a decryption circuit separate from the error correction circuit, as *Oishi* clearly teaches separate circuits. Combining the decryption circuit with the error correction circuit in a single circuit would be contrary to the teachings of *Oishi* and, thus, improper.

*Schneier* is cited for the aspect of teaching that encryption and decryption can be performed in a hardware circuit. *Schneier*, however, does not make up for the above-discussed deficiencies in *Hirofani* and *Oishi*.

Accordingly, it would not have been obvious to a person having ordinary skill in the art to combine the teachings of *Hirofani*, *Schneier* and *Oishi* in the manner suggested by the Examiner. The teachings of *Oishi* teach completely away from such a combination as noted above. Therefore, the references do not teach or suggest all the features of independent claims 1, 3, 6 and 8 as claimed and, therefore, the rejection under 35 USC §103(a) is improper.

For at least the above reasons, withdrawal of the rejection is respectfully requested.

## **II. REJECTION OF CLAIMS 2 AND 5 UNDER 35 USC §103(a)**

Claims 2 and 5 stand rejected under 35 USC §103(a) based on *Hirofani*, *Oishi* and *Schneier* in further view of *Qualline* and *Ooi et al.* Applicants respectfully traverse this rejection for at least the following reasons.

Claims 2 and 5 depend from one of the above independent claims and, therefore, can be distinguished from the cited art for at least the same reasons.

Accordingly withdrawal of the rejection of claims 2 and 5 is respectfully requested.

## **III. CONCLUSION**

Accordingly, claims 1-3 and 5-9 are believed to be allowable and the application is believed to be in condition for allowance. A prompt action to such end is earnestly solicited.

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Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Respectfully submitted,

RENNER, OTTO, BOISSELLE & SKLAR, LLP

By /Kenneth W. Fafrak/  
Kenneth W. Fafrak, Reg. No. 50,689  
Mark D. Saralino, Reg. No. 34,243

1621 Euclid Avenue  
Nineteenth Floor  
Cleveland, Ohio 44115  
PH: (216) 621-1113  
FAX: (216) 621-6165  
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